AMENDMENTS TO THE CLAIMS

Claims 15-18 and 24-31 were pending. Claims 24-27 have been amended, without acquiescence in cited basis for rejection or prejudice to pursue in a related application. No new matter has been added. A complete listing of the current pending claims is provided below and supersedes all previous claims listing(s).

1-14. (Canceled)

15. (Previously Presented) An apparatus comprising:

means for dividing p pins of an integrated circuit into n groups;

means for logically associating the pins of each group through an ExOR matrix; and

means for driving a plurality of scan chains in the integrated circuit with the logically associated pins, wherein the plurality of scan chains are driven by ExORing the pins from the n groups, and the ExOR matrix is configured such that the number of pins logically associated through the ExOR matrix is less than the number of scan chains coupled to the ExOR matrix.

16. (Original) The apparatus of claim 15, wherein said means for logically associating the pins further comprises:

means for generating (p/n)^n logical associations, where p is the number of pins, and n is the number of groups of pins.

17. (Original) The apparatus of claim 15, wherein the number of scan chains is equal to the number of logical associations.

18. (Original) The apparatus of claim 15, wherein the ExOR matrix has n dimensions.

19-23. (Canceled)

24. (Currently Amended) A computer readable memory ~~storage medium~~ having stored thereon a computer program which, when executed by a processor, causes the execution of a process, the memory ~~medium~~ comprising:

code for dividing p pins of an integrated circuit into n groups;

code for logically associating the pins of each group through an ExOR matrix;

code for driving a plurality of scan chains in the integrated circuit with the logically associated pins, wherein the plurality of scan chains are driven by ExORing the pins from the n

groups, and the ExOr matrix is configured such that the number of pins logically associated through the ExOR matrix is less than the number of scan chains coupled to the ExOR matrix; and

code for storing a result of a logical operation performed by the ExOR matrix.

25. (Currently Amended) The memory ~~medium~~ of claim 24, wherein said code for logically associating the pins further comprises:

code for generating (p/n)^n logical associations, where p is the number of pins, and n is the number of groups of pins.

26. (Currently Amended) The memory ~~medium~~ of claim 24, wherein the number of scan chains is equal to the number of logical associations.

27. (Currently Amended) The memory ~~medium~~ of claim 24, wherein the ExOR matrix has n dimensions.

28. (Previously Presented) A method comprising:

dividing p pins of an integrated circuit into n groups;

logically associating the pins of each group through an ExOR matrix; and

driving a plurality of scan chains in the integrated circuit with the logically associated pins, wherein the plurality of scan chains are driven by ExORing the pins from the n groups, and the ExOR matrix is configured such that the number of pins logically associated through the ExOR matrix is less than the number of scan chains coupled to the ExOR matrix.

29. (Previously Presented) The method of claim 28, wherein said logically associating the pins further comprises:

generating (p/n)^n logical associations, where p is the number of pins, and n is the number of groups of pins.

30. (Previously Presented) The method of claim 28, wherein the number of scan chains is equal to the number of logical associations.

31. (Previously Presented) The method of claim 28, wherein the ExOR matrix has n dimensions.

32-46. (Canceled).